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APPLICATION FOR LETTERS PATENT

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Field Effect Transistors, Integrated Circuitry, Methods Of Forming Field Effect Transistor Gates, And Methods Of Forming Integrated Circuitry

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TECHNICAL FIELD

This invention relates to field effect transistors, to integrated circuitry, to methods of forming field effect transistor gates, and to methods of forming integrated circuitry.

BACKGROUND OF THE INVENTION

One aspect of semiconductor wafer processing includes making buried contacts to field effect transistor gate lines. A conventional gate line typically comprises a gate dielectric layer and a conductively doped polysilicon layer (typically n+ doped) and an overlying silicide layer (i.e., WSi_X). These gates are typically fabricated by deposition or provision of these three layers over a semiconductor substrate, followed by collectively patterning these layers with photoresist to form the desired gate outlines. An insulative capping material might also be provided over the silicide layer prior to patterning to form the conductive portions of the gate line. Transistor gates might also be fabricated using damascene methods, and also above or below a thin film semiconductor layer such as in fabrication of semiconductor-on-insulator circuitry which might be top or bottom gated.

A thick insulating layer, such as borophosphosilicate glass, is typically provided over the resultant transistor and provided with an upper planar surface. Contact openings can then be etched through the insulating layer to the outer conductive portion of the transistor gates, as well as to other substrate areas. The openings are filled with conductive plugging material. Metal or conductively doped semiconductive material, such as polysilicon, are example materials.

In certain applications, it may be desirable that the conductive plugging material be a semiconductive material having opposite type conductivity enhancing dopant impurity as compared to the conductivity type impurity within the semiconductive material of the gate. For example where the gate is heavily doped to achieve conductivity with n-type material, in some applications it might be desirable to provide a conductively doped contact plug to that gate with p-type material. Unfortunately, the different dopants types can easily cross-diffuse relative to one another through the silicide which can lead to no conductive connection. One prior art solution to avoiding this diffusion is to initially line the contact opening with a very thin layer of an electrically conductive diffusion barrier material, such as TiN. Subsequently, the remaining portion of the opening is filled with conductively doped polysilicon to provide the desired electrical connection with the transistor gate.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 3.

Fig. 5 is a diagrammatic sectional view of an alternate embodiment semiconductor wafer fragment to that depicted by Fig. 4.

Fig. 6 is a diagrammatic sectional view of another alternate embodiment semiconductor wafer fragment in accordance with the invention.

SUMMARY OF INVENTION

The invention includes field effect transistors, integrated circuitry, methods of forming field effect transistor gates, and methods of forming integrated circuitry. In one implementation, a field effect transistor includes a pair of source/drain regions having a channel region positioned therebetween. A gate is positioned operatively proximate the

channel region, and includes conductively doped semiconductive material, a silicide layer and a conductive diffusion barrier layer.

In another implementation, integrated circuitry comprises a field effect transistor having a gate, a gate dielectric layer, source/drain regions and a channel region. The gate comprises semiconductive material conductively doped with a conductivity enhancing impurity of a first type and a conductive diffusion barrier layer. Insulative material is provided proximate the gate, and includes semiconductive material therein which is in electrical connection with the gate. Such semiconductive material is conductively doped with a conductivity enhancing impurity of a second type. The conductive diffusion barrier layer of the gate is provided between the gate semiconductive material and the semiconductive material provided within the insulative material.

A method of forming a field effect transistor gate includes forming a layer of conductively doped semiconductive material over a substrate, forming a layer of a conductive silicide over the substrate, and forming a conductive diffusion barrier layer over the substrate. Portions of the semiconductive material layer, the silicide layer and the conductive diffusion barrier layer are removed to form a transistor gate comprising the semiconductive material, the conductive silicide and the conductive diffusion barrier layer.

Other aspects are disclosed and claimed.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

The discussion initially proceeds with reference to a preferred embodiment of Figs. 1-4. Referring to Fig. 1, a semiconductor wafer fragment 10 in one embodiment comprises a bulk monocrystalline silicon substrate 12. A gate dielectric layer 14 (i.e., thermally grown silicon dioxide having a thickness of from 50 to 90 Angstroms) is formed over substrate 12. A layer 16 of conductively doped semiconductive material is formed over substrate 12 and gate dielectric layer 14, such as by chemical vapor deposition of polysilicon wherein the dopant is provided *in situ*. An example dopant is any suitable n-type dopant deposited to an example concentration of at least 5 X 10^{20} atoms/cm^3. A layer 18 of a conductive silicide is formed over the substrate and doped semiconductive material layer 16. Example preferred materials are refractory metal silicides, such as WSi_x and $TiSi_x$. Such can be formed by chemical vapor deposition, refractory metal layer deposition followed by a silicidation anneal, or other manner. A preferred thickness for layer 18 is from 800 to 1400 Angstroms.

A conductive diffusion barrier layer 20 is formed over the substrate and, in this example, over silicide layer 18. Example materials include titanium compounds and tungsten compounds. Preferred example materials are TiN, TiO_xN_y, W_xN_y and TiW_xN_y, for example *deposited*

by chemical vapor deposition to a thickness of from 100 to 300 Angstroms. Accordingly in this embodiment, the conductive diffusion barrier layer is provided over both silicide layer 18 and doped semiconductive material layer 16, and in contact with silicide layer 18. Further, conductive diffusion barrier layer 20 is not in contact with semiconductive material layer 16.

An insulative capping layer 22 is preferably formed over the conductive gate materials, with an example being SiO_2 or Si_3N_4 deposited to a thickness of from 1,500 to 2,500 Angstroms. A masking layer, such as deposited photoresist, is formed over the underlying layers and selectively exposed to light and developed, forming a photoresist mask 24 in the shape of a desired transistor gate line.

Referring to Fig. 2, portions of semiconductive material layer 16, silicide layer 18, conductive diffusion barrier layer 20 and insulating layer 22 have been removed to form a transistor gate 26 comprising the above-described conductive materials. Such removal is preferably by etching away unmasked portions by conventional etching techniques, thereby forming a transistor gate initially beneath masking layer 24. Such is shown as having been removed in Fig. 2. Gate 26 defines or is positioned over and operatively proximate a channel region 28, here formed within bulk semiconductor substrate 12.

Referring to Fig. 3, lightly doped drain regions 30 are formed within bulk substrate 12 laterally outward of gate 26, followed by deposition and anisotropic etching of an insulative material to form

spacers 32. A pair of source/drain regions are formed within substrate 12, with channel region 28 accordingly being positioned therebetween.

Referring to Fig. 4, an insulative layer 36 is formed over the substrate, with an example being borophosphosilicate glass (BPSG) deposited to a thickness of 10,000 Angstroms. Such provides but one example of providing insulative material which is received proximate gate 26. Layer 36 is preferably planarized, as shown. An opening 38 is formed into insulative layer 36, and all the way to a conductive portion of gate 26, as shown. Semiconductive material conductively doped with a conductivity enhancing impurity opposite in type to that used to dope material 16 is formed within the opening. A preferred technique is chemical vapor deposition with *in situ* doping, followed by planarization such as chemical-mechanical polishing to produce the illustrated plug 40 of semiconductive material within opening 38. Such provides but one example of providing conductively doped semiconductive material within electrically insulative material 36, which is proximate gate 36, and in electrical connection with gate 36. Conductive diffusion barrier layer 20 of gate 26 is accordingly received between or intermediate semiconductive material 16 of gate 26 and semiconductive material 40 within opening 38. Fig. 4 illustrates plugging material 40 as comprising p+ doped material, with the semiconductive polysilicon material of layer 16 being n+ doped. Such could of course be reversed. Alternately, the conductivity types could be the same.

Further considered, silicide layer 18 might not be included in certain aspects of the invention, which is intended only to be limited by the accompanying claims appropriately interpreted in accordance with the Doctrine of Equivalents. Where a silicide layer is utilized, preferably the silicide layer and conductive diffusion barrier layer comprise a common metal. For example where the silicide is WSi_x, a preferred barrier layer material is one or more of W_xN_y and TiW_xN_y. Where the silicide layer is $TiSi_x$, a preferred barrier layer material is one or more of TiN, TiO_xN_y, and TiW_xN_y. The barrier layer and silicide layer are preferably deposited in the same chamber.

The above-described first embodiment provides a construction whereby semiconductive material 40 within insulating material 36 contacts conductive diffusion barrier layer 20 of gate 26, but not silicide layer 18. Further, conductive diffusion barrier layer 20 is in contact with silicide layer 18 and not semiconductive material layer 16. Yet, conductive diffusion barrier layer 20 is received over both silicide layer 18 and semiconductive material layer 16. Fig. 5 illustrates but one embodiment alternate to that of Fig. 4. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated by the suffix "a" or with different numerals. Here, conductive diffusion barrier layer 20a is provided immediately over and in contact with semiconductive material 16, and silicide layer 18a is provided immediately over barrier layer 20a. Accordingly, conductive diffusion barrier layer 20a is in contact with both semiconductive

material 16 and silicide layer 18a. Further, silicide layer 18a is received over conductive diffusion barrier layer 20a. Further, semiconductive material 40 within insulative material 36 does not contact conductive diffusion barrier layer 20a of gate 26a, but does contact silicide layer 18a. In both above-described embodiments, opening 38 within insulating material 36 is most preferably substantially or essentially void of any conductive diffusion barrier layer material, thus potentially simplifying processing for example over that disclosed above as prior art.

The above-described embodiments depict exemplary implementations associated with bulk substrate processing. Processing is also contemplated in accordance with the invention with semiconductor-on-insulator layers or other layers, and with the gates and contact plugging semiconductive material being received variously or beneath such semiconductor-on-insulator layers.

Fig. 6 illustrates a further exemplary implementation of the invention. A semiconductor wafer fragment 60 comprises a bulk monocrystalline silicon substrate 62 having shallow trench oxide isolation regions 64 formed therein. An n+ diffusion region 66 and a p+ diffusion region 68 are formed intermediate pairs of isolation regions 64, as shown. A gate construction 70, such as a gate 26 in the above-described first embodiment, is shown provided over the far-right illustrated isolation region 64. A planarized insulating layer 72 is formed over the substrate, and includes a plurality of contact

openings 74, 76, and 78 formed therein to diffusion region 66, diffusion region 68, and gate 70, respectively. Opening 74 is plugged with n+ conductively doped semiconductive material 80 for making electrical connection with n+ diffusion region 66. Openings 76 and 78 are plugged with p+ conductively doped semiconductive material 82.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.